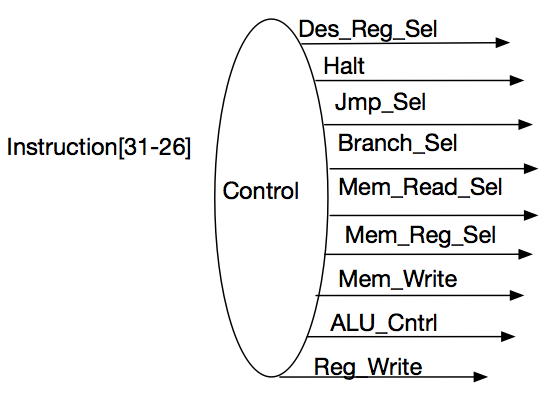
#### Control Unit

jx755

#### 1.1 inplementation

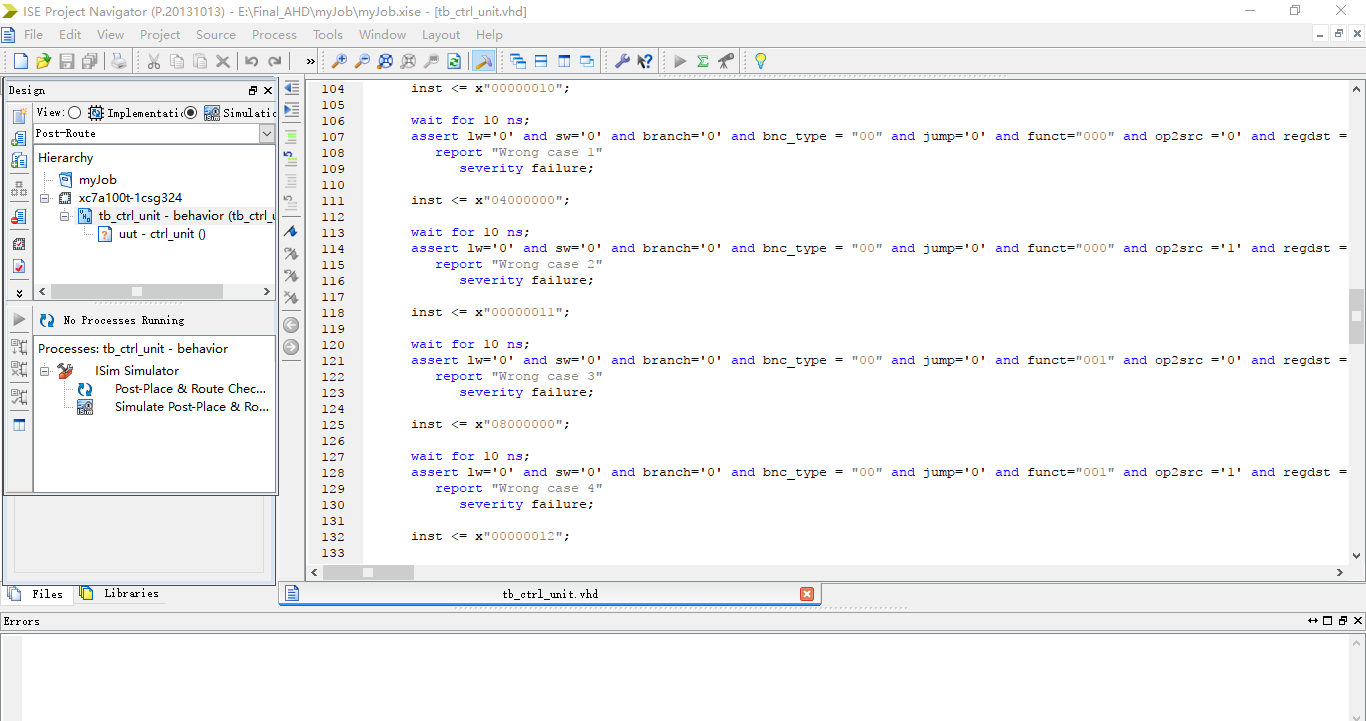
The control unit of the block diagram examines the instruction opcode bits [31 – 26] and decodes the instruction to generate control signals to be used in the additional modules. The Dst\_Reg\_Del determines which register will be selected to be written into the register file. The Jmp\_Sel control signal selects the jump address to be sent to the PC. The Branch\_Sel is used to select the branch address to be sent to the PC. The Mem\_Read\_sel control signal is asserted during a load instruction when the data memory is read to load a register with its memory contents. The Mem\_Reg\_select control signal determines if the ALU result or the data memory output is written to the register file. The MEM\_Write control signal is asserted when during a store instruction when a registers value is stored in the data memory. The ALU\_Cntrl control signal determines if the ALU second operand comes from the register file or the sign extend. The Reg\_Write control signal is asserted when the register file needs to be written.



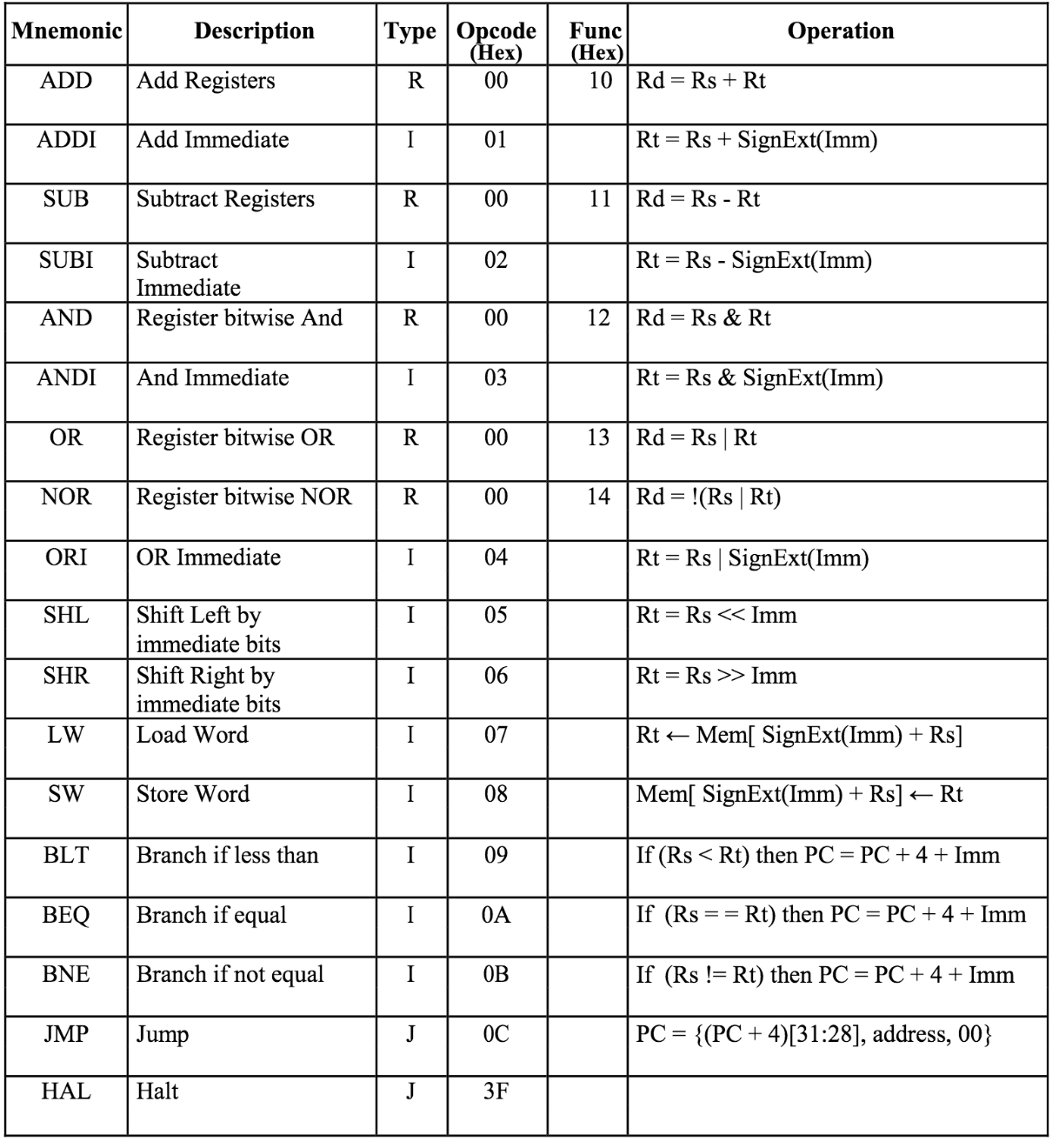
We tested all 18 instrutions and checked if the output controll signals are correct.

##### 1.2 testbench

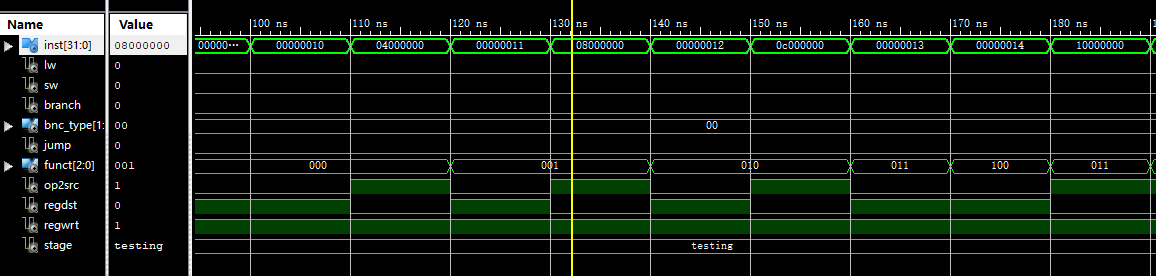
For each condition, I make one instruction to test correctness(bits unused is set to be zero) and used ‘assert’ statement to check the output automatically (see tb\_ctrl\_unit.vhd for details). The stage signal would change to FINISH only when all test cases passed, otherwise, the simulation would stop with severity level ‘failure’.



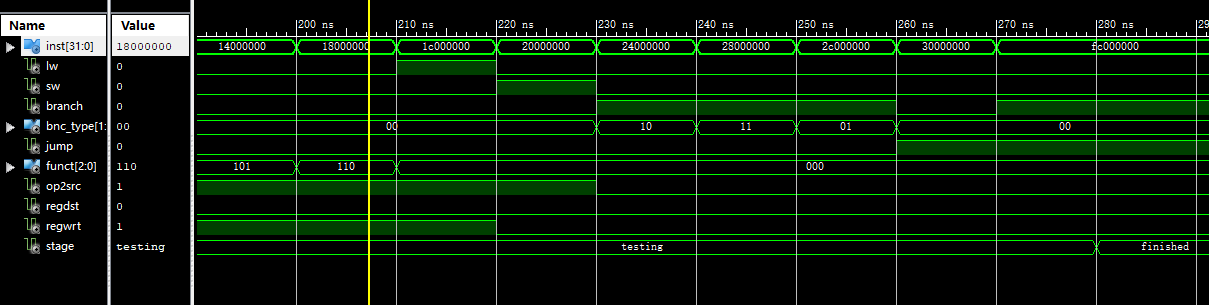
And the order of test instructionts are according to the instrucionts needed as:



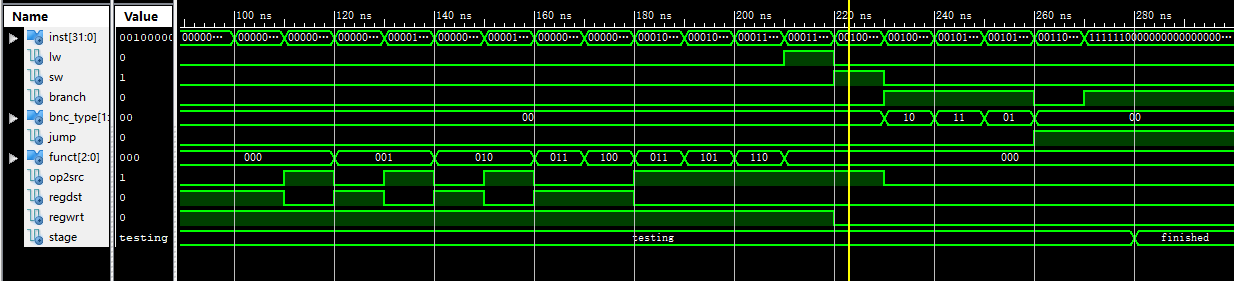
##### 1.3 Functional Simulation



1.3.1 Testing first 9 conditions

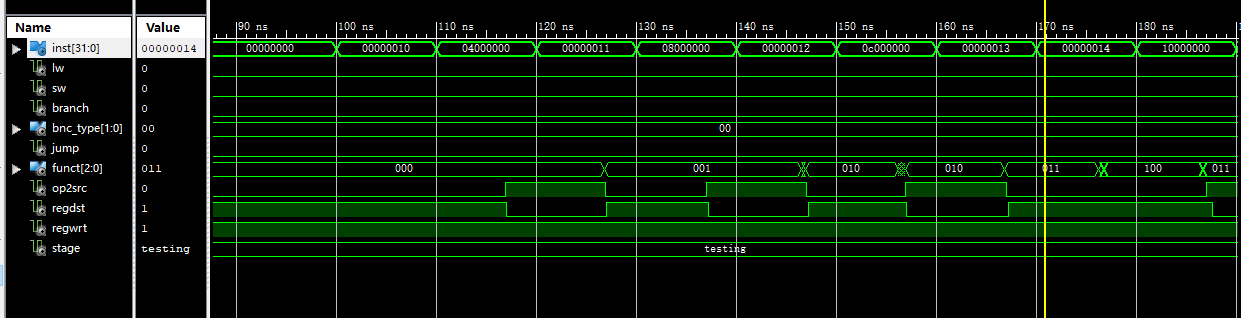


1.3.2 Testing latter 9 conditions

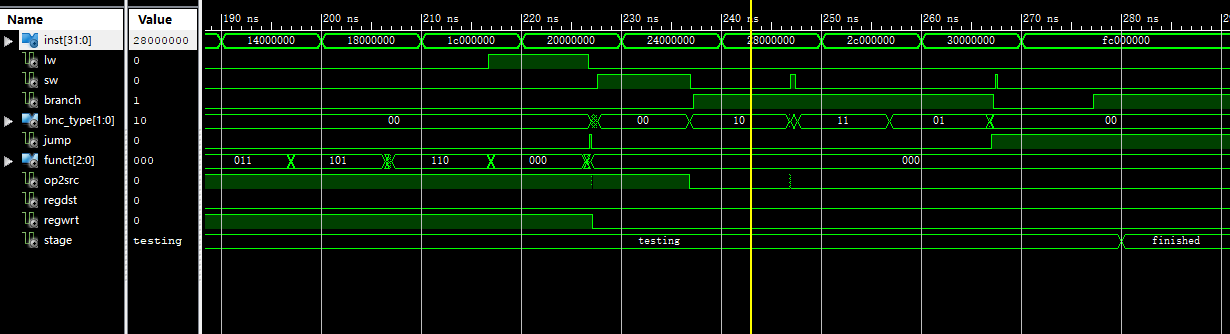


1.3.3 An overview with all cases passed.

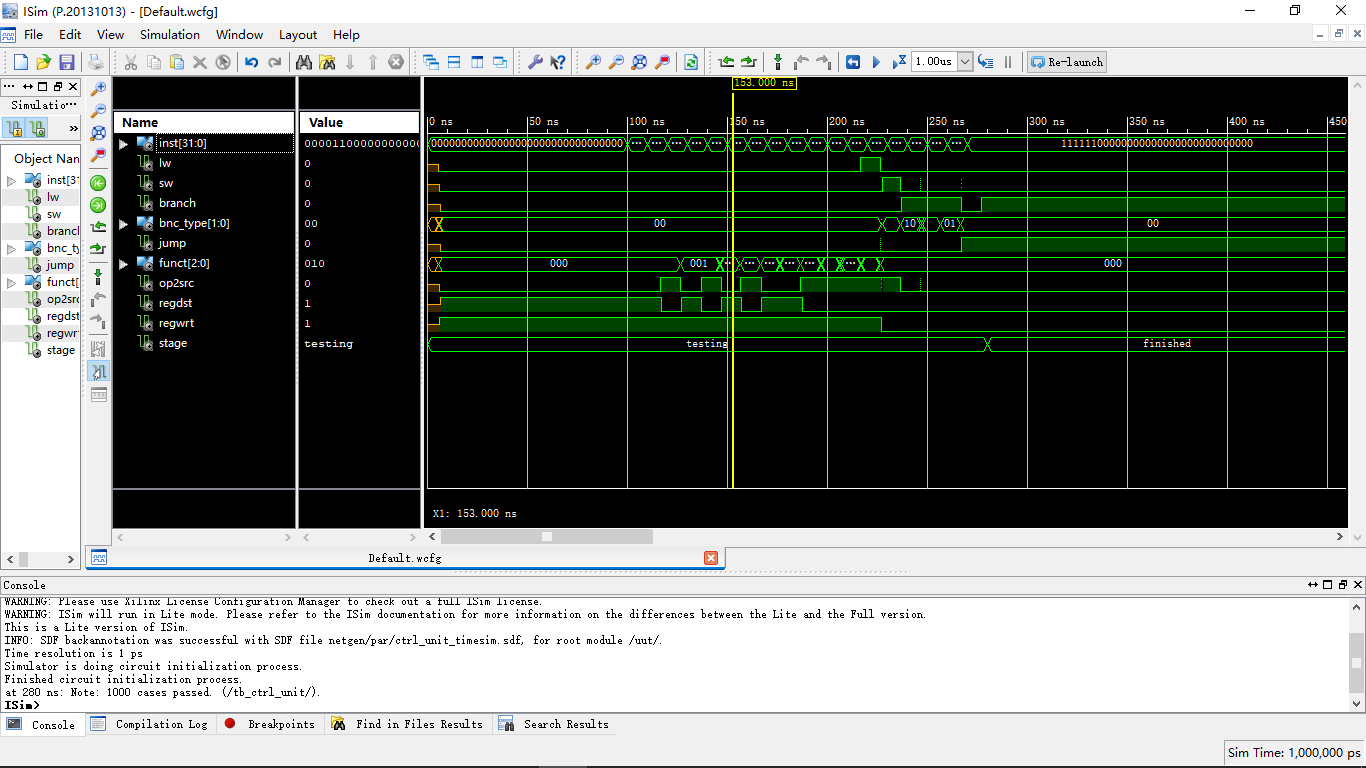
##### 1.4 Timing Simulation



1.4.1 Testing first 9 conditions



1.4.2 Testing latter 9 conditions



1.4.3 An overview with all cases passed.

1.5 timing analysis

|  |  |
| --- | --- |
| Critical path delay | 2.356 ns |
| Highest frequency | MHz |

Try many time after google, no timing report shows: The clock report is not displayed in the non timing-driven mode.